Title: Verilog-Based Secure Voting Machine

Abstract:

This project introduces a straightforward and secure electronic voting machine (EVM) designed using Verilog Our focus is on making voting secure and user-friendly. The Verilog code ensures a tamper-resistant design, safeguarding against common vulnerabilities. We implement advanced encryption techniques to secure communication between different parts of the system, ensuring the integrity of the voting process. The design is flexible, making it adaptable to various election needs. The user interface is kept simple for easy voting and verification. With optimized Verilog code, the system is efficient, reliable, and power-conscious, providing a practical solution for transparent and secure electronic voting.

Outcomes:

1. A secure voting machine is designed by Verilog
2. All functionality is designed and verified.
3. By understanding practical experience of voting machine by our theoretical knowledge